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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	10/066,188
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2664 2825
				Examiner Name	LIN, SUN JAMES
Sheet	1	of	1	Attorney Docket Number	SPLX.P0095

IDC-US Ref -12				U.S. PATENT DOCUMENTS	
Examiner Initials	Cite No.	U.S. Patent Document Number Kind Code* (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
Jed	1.	5,311,442	05-10-1994	Fukushima	
	2.	5,526,276	06-11-1996	Cox et al	
	3.	5,752,000	05-12-1998	McGeer et al	
	4.	6,086,626	07-11-2000	Jain et al	
	5.	6,102,964	08-15-2000	Tse et al	
	6.	6,134,705	10-17-2000	Pedersen et al	
	7.	2001/013113	08-09-2001	Matsunaga	
	8.	6,297,772	10-02-2001	Phillips et al	
	9.	6,336,208	01-01-2002	Mohan et al	
	10.	6,473,884	10-29-2002	Ganai et al	
	11.	6,490,717	12-03-2002	Pedersen et al	
	12.	6,546,539	04-08-2003	Lu et al	

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Examiner Signature	<i>James Sun</i>	Date Considered	9-1-05
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IDC-US Ref -7 U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	U.S. Patent Document Number Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JSA	1.	5,519,630	05-21-1996	Nishiyama et al.	
	2.	5,537,341	07-16-1996	Rose et al. Roes, et al	
	3.	5,696,974	12-09-1997	Agrawal et al.	
	4.	5,574,441	05-19-1998	Tokunoh et al. 5,754,441	
	5.	5,787,010	07-28-1998	Schaefer et al.	
	6.	6,023,566	02-08-2000	Belkhale et al.	
	7.	6,301,696	B1 11-09-2001	Lien et al.	

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ³
JSA	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.	
JSA	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.	

Examiner Signature	<i>James Sun Lin</i>	Date Considered	9-1-05
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